CLAIMS

1. An active matrix device, comprising an array of matrix elements wherein the matrix elements each have at least one storage node having a capacitance for storing data dynamically in the form of charge stored on the capacitance and the matrix elements further include refresh circuitry for refreshing the data stored on the storage node.

2. An active matrix device according to claim 1 wherein the refresh circuitry includes a temporary storage circuit for storing the data on the at least one storage node and a storage node drive circuit for driving the storage node in accordance with the data stored on the temporary storage circuit.

3. An active matrix device according to claim 1 or 2 wherein the storage node drive circuit includes an inverter for driving the at least one storage node with the inverse of the data stored on the temporary storage circuit.

4. An active matrix device according to any preceding claim further comprising a refresh line for activating the refresh circuitry to refresh the storage node.

5. An active matrix device according to any preceding claim wherein the or each storage node comprises a capacitor.

6. An active matrix device according to any preceding claim wherein each matrix element includes an address switch controlled by an address line and connected between a column line and the at least one data storage node, a storage switch connecting the storage node to the temporary storage circuit and a refresh switch connecting the storage node to the storage node drive circuit, the storage switch and the refresh switch having control terminals connected to a common refresh line for switching between a first

setting in which the storage switch is open and the refresh switch is closed and a second setting in which the storage switch is closed and the refresh switch is open.

7. An active matrix device according to any preceding claim wherein the matrix elements each include a plurality of data storage capacitances for storing a plurality of bits of data per matrix element.

8. An active matrix device according to claim 7 including a plurality of row address lines controlling a plurality of address thin film transistors connected to respective data storage capacitances to select one or more of the data storage capacitances.

9. An active matrix device according to claim 8 wherein the plurality of address thin film transistors are connected to a common drive line connected through a select transistor to the column line, wherein the select transistor is controlled by a select line.

10. An active matrix device according to claim 9 further comprising a refresh line controlling the refresh circuit to connect the refresh circuitry to the common drive line to refresh the selected data storage capacitor.

11. An active matrix device according to any preceding claim wherein the refresh circuitry includes a pair of cross-coupled inverters.

12. An active matrix device according to claim 7 wherein:

each matrix element includes a plurality of register units connected in series, each register unit including a data storage node, and register units connected to subsequent register units including a drive means for driving the next register unit; and

at least one clock line is provided for controlling the transmission of data along the series of register units.

13. An active matrix device according to claim 12 wherein in each register unit the output of the drive means is connected back to the storage node for refreshing data stored on the storage node so that the drive means constitutes the refresh circuit.

14. An active matrix device according to any preceding claim wherein the matrix elements are display pixels for displaying an image pixel in accordance with data stored on the data storage node.

15. An active matrix device according to any preceding claim wherein the matrix elements are pixel electrodes for controlling liquid crystal.

16 A method of operating an active matrix device having matrix elements including capacitative storage nodes, comprising

storing image data as charge on the storage nodes and

operating the active matrix device in a refresh mode including displaying the stored image data, and periodically applying refresh signals to refresh circuitry within the matrix elements to cause the refresh circuitry to refresh the image data stored on the storage nodes.

17. A method according to claim 16 further including operating the active matrix device in a normal mode including regularly addressing the matrix elements with fresh video information and displaying the video information.